

FORM PTO-892 (REV. 2-92)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER	
NOTICE OF REFERENCES CITED						APPLICANT(S)			
Tsang et al.									
U.S. PATENT DOCUMENTS									
•		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE		
A		6,215,442	5/29/99	Bulacev et al.	257	350			
B		4,914,028	4/13/90	Blanchard	257	353			
C									
D									
E									
F									
G									
H									
I									
J									
K									
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•		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
L		5,119,775	5/91	Japan	Sakamoto	257	352		
M									
N									
O									
P									
Q									
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)									
R									
S									
T									
U									
EXAMINER	DATE								
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)									

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED				APPLICANT(S)		
				A. Tsang et al		

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*	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING ANALYST	SEARCHER
*	A 5 1-08437	8/92	Jain et al	437	40		
*	B 4 5 87712	5/86	Kaliga	437	6		
*	C 5 089434	2/92	Hilfinger	437	41		
*	D 5 017522	5/91	Mayer et al	437	40		
*	E 4 325073	4/82	Hughes et al	11	11		
*	F 5 108937	4/92	Jain et al	11	11		
*	G 4 713358	12/87	Bulat et al	437	6		
*	H 4 656076	4/87	Vetanen et al	437	41		
I							
J							
K							

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*	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHEETS DWG. NO. PP. NO. SPEC.
L							
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Q							

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*	REFERENCE						
*	R Chang, <u>Bi-directional Gate Bipolar Transistor (IGBT) with a Trench Plate Structure</u> , IEDM Tech Digest, 1987, pp. 674-677.						
*	S Shenai, <u>Optimum Low Voltage IGBT and Power Switches Fabricated Using Implanted Ion-implanted MOS Technologies</u> , IEDM Tech Digest, 1991, pp. 893-897.						
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*	U Shenai, <u>A 55-V, 0.2-ms² Vertical Trench Power MOSFET</u> , Electron Dev. Lett. EDL-12, 703, Mar. 1991, pp. 108-110.						

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(See Manual of Patent Examining Procedure, section 201.05 (a).)